, . . . Applicant(s)/Patent Under Reexamination Application/Control No. 10/075,464 KAWANAKA, SHIGERU Notice of References Cited Art Unit Examiner Page 1 of 1 2826 Kevin Quinto

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	Α	US-4,722,910	02-1988	Yasaitis, John A.	438/297
X	В	US-5,162,880	11-1992	Hazama et al.	365/184
X	C	US-5,494,857	02-1996	Cooperman et al.	438/437
X	D	US-5,736,435	04-1998	Venkatesan et al.	438/151
X	Е	US-6,534,373	03-2003	Yu, Bin	438/372
	F	US-			
	G	US-			
	Н	US-			
	-	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	Ν					
	0					
	Ρ					
	σ					
	R					
	s					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Wolf, "Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," 1990, Lattice Press, p.12-13			
	٧				
	w				
	x				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.